

What is Claimed is:

1 1. A zero-generating apparatus for use with an instruction set architecture
2 without an r0 register, comprising:
3 a physical zero register which reads as a zero value;
4 a Register Alias Table (RAT) for storing an instruction register map; and
5 a Zeroing Instruction Logic (ZIL) unit for detecting a zeroing instruction
6 and modifying said RAT with a pointer to said physical zero register.

1 2. An apparatus in accordance with claim 1, wherein:
2 said physical zero register is a read only memory (ROM).

1 3. An apparatus in accordance with claim 1, wherein:
2 said ZIL unit detects said zeroing instruction in a trace cache line.

1 4. An apparatus in accordance with claim 3, further comprising:
2 an r0 register field logically coupled to said trace cache line for mapping to
3 said physical zero register.

1 5. An apparatus in accordance with claim 3, wherein:
2 said RAT and said trace cache line are logically coupled to a renaming unit
3 for maintaining said pointer to said physical register.

1 6. An apparatus in accordance with claim 3, wherein:
2 said ZIL unit deletes said zeroing instruction from said trace cache line.

1 7. An apparatus in accordance with claim 6, wherein:
2 said ZIL unit modifies a subsequent instruction, where said subsequent
3 instruction is logically coupled to said zeroing instruction within said trace cache line.

1 8. An apparatus in accordance with claim 7, wherein:
2 said ZIL unit modifies said subsequent instruction with an immediate
3 source of zero.

1 9. An apparatus in accordance with claim 1, wherein:
2 said zeroing instruction is an exclusive or (XOR).

1 10. An apparatus in accordance with claim 1, wherein:

2 said zeroing instruction is a subtraction (SUB).

1 11. An apparatus in accordance with claim 1, wherein:

2 said zeroing instruction is a multiply (MUL).

1 12. An apparatus in accordance with claim 1, wherein:

2 said zeroing instruction is a move (MOV).

1 13. An apparatus in accordance with claim 7, wherein:

2 said ZIL unit transforms said subsequent instruction to a MOV instruction.

1 14. A zero-generating apparatus for use with a microprocessor, comprising:

2 a physical zero register which reads as a zero value;

3 a Zeroing Instruction Logic (ZIL) unit for reading a plurality of instructions

4 and detecting and modifying a zeroing instruction within said plurality of instructions;

5 where said ZIL unit deletes said zeroing instruction and sets a pointer to

6 said physical zero register in place of said deleted zeroing instruction; and

7 where said ZIL unit modifies instructions dependent on said deleted zeroing
8 instruction.

1 15. An apparatus in accordance with claim 14, wherein:
2 said ZIL unit modifies instructions dependent on said deleted zeroing
3 instructions with an immediate source of a value when both occur with a single trace
4 cache line.

1 16. An apparatus in accordance with claim 14, wherein:
2 said ZIL unit modifies instructions dependent on said deleted zeroing
3 instructions with a renameable pointer.

1 17. A method of zero-generating with an instruction set architecture with an r0
2 register, comprising:
3 detecting a zeroing instruction;
4 deleting said zeroing instruction;
5 identifying a subsequent instruction using said zeroing instruction; and
6 modifying said subsequent instruction.

1 18. A method in accordance with claim 17, further comprising:
2 pointing to a physical zero register where said subsequent instruction is not
3 within a common trace cache line.

1 19. A method in accordance with claim 17, wherein:
2 modifying said subsequent instruction involves replacing instruction
3 sources.

1 20. A method in accordance with claim 17, wherein:
2 modifying said subsequent instruction involves using a move (MOV)
3 instruction.

1 21. A method in accordance with claim 17, wherein:
2 said subsequent instruction is modified in response to its location in a trace
3 cache relative to said zeroing instruction.